REMARKS

After entry of this Amendment, claims 4-13, 18, 19, 21-24, 31-42, 44-46, and 51-71 will be pending in this application. Claim 31 has been amended to clarify the scope of the invention. Support for the amendment may be found throughout the Specification, at least in Figures 3 and related text, and in the originally filed claims.

Telephone Conference

The undersigned wishes to thank Examiner Tran for his time and courtesy during the telephonic interview that took place with Steven Frank and Daniel Shepard on April 22, 2009. The following discussion is intended to constitute a proper recordation of such interviews in accordance with MPEP §713.04, and also to provide a full response to the Office Action mailed on December 24, 2008.

Rejection of Claims under 35 U.S.C. § 112

Claims 4-13, 18, 19, 21-24, 31-42, 44-46, and 51-71 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that applicant regards as the invention. In particular, the Examiner requested explanation of the phrase "directly connected." Applicant directs attention to Figs. 3-5, 13, and 14, where rectifiers D9 – D32 in the address circuitry (grouped as L) are directly connected (without intervening circuitry) to conductive lines X-000 – X-111. Applicant submits that this disclosure is sufficient to satisfy the requirements of 35 U.S.C. § 112, second paragraph.

Further, in response to the Examiner's helpful suggestion, Applicant provides the following chart, which includes non-limiting illustrative examples of elements of amended independent claim 31. It should be understood that this chart is exemplary and not limiting, and there is no intent to confine the claims to the features enumerated below. Further, Applicant notes that the features described below are present in the elected species of Fig. 14; references to Fig. 3 are purely for convenience, as Fig. 3 contains more comprehensive labeling of the features in question.

Element/Feature	***Illustrative Example***
First and second sets of conductive address lines	Fig. 3, elements P and O
Pattern of information-defining nonlinear elements	Fig. 3, element K
Address circuitry	Fig. 3, elements L and N
First pattern of rectifiers	Fig. 3, element L
First set of address signal lines	Fig. 3, element N

Rejection of Claims under 35 U.S.C. § 102

Claim 31 is rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 3,701,119 to Waaben et al. ("Waaben"). Waaben appears to disclose a transistor and diode-based switch for use with semiconductor memories. *See* Waaben, Fig. 1 and related text. The examiner relies on Waaben to teach all of the limitations of independent claim 31.

However, Waaben's diodes 16 (part of control circuit 12) and 30 are not part of address circuitry, as required by amended independent claim 31. Waaben discloses that "control circuitry 12 corresponding to the digit line 14 coupled to the selected memory cell 36, is rapidly turned on and operated in saturation." *See* Waaben, column 3, lines 55-58 (emphasis added). That is, a particular control circuit 12 is operated once a particular digit line 14 has already been addressed (i.e., selected) by an external addressing means (not described).

Further, even if control circuit 12 including diodes 16 and 30 were address circuitry, it does not disable all but one of a first set of conductive lines, as required by amended independent claim 31. Rather, once a digit line 14 is selected (by means undisclosed in Waaben), this "causes forward conduction through diode 16 and 18 to rapidly cease" and "cut[s] off forward conduction in diode 30." *See* Waaben, column 3, lines 63-65 and column 4, lines 40-45. Indeed, the point of Waaben's invention is a "diode switch" on a digit line that "acts as a short circuit in the reverse direction until all of the minority carriers are dissipated … then automatically acts as an open circuit." *See* Waaben, column 2, lines 14-20. Thus, if anything, it is the components on the *selected* line that are disabled by control circuit 12, not all of the other digit lines.

Finally, Waaben also fails to teach or suggest presence or absence of a nonlinear element connection at a storage location defining a bit state at the location, as required by amended independent claim 31. Rather, Waaben's bit information is represented by "charge stored in the

memory cell," where memory cells are present at each intersection in his array. *See* Waaben, column 1, lines 46-47 and Fig. 1. Waaben does not specify the nature of the memory cells.

Applicants submit that amended independent claim 31 and claims dependent therefrom are allowable over the cited art for at least these reasons.

Claim 31 is further rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 4,608,672 to Roberts et al. ("Roberts"). Roberts appears to disclose a semiconductor memory with an address decoder in the center of the data field. *See* Roberts, column 1, lines 10-16. The Examiner relies on Roberts to teach all of the limitations of independent claim 31.

However, Roberts' diodes 220, 222, 230, 232 are not and cannot be part of address circuitry in which application of an address to a first set of address signal lines causes a first pattern of rectifiers to disable all but one of a first set of conductive lines, as required by amended independent claim 31. Rather, Roberts discloses that these diodes are part of select means 42 and 44, and "are adapted to select only the [entire] left or right memory array," not an individual line therein. *See* Roberts, column 5, lines 57-63.

Further, Roberts' address decode means 12 features NAND gates 50, 52 connected directly to his wordlines 58, 60. *See* Roberts, Figs. 2 and 3 and related text. Roberts does not teach or suggest a first pattern of rectifiers directly connected between a first set of conductive lines and a first set of address signal lines, as required by amended independent claim 31.

Finally, the diodes in Roberts' address decoder 12 — e.g., Schottky diodes 197 – 199 of Fig. 3 — connect only to the NAND gates and internal $\overline{WL}$ lines (e.g., line 54) and do not connect to left memory array 20 or right memory array 22. *Ibid.* Rather, the diodes in address decoder 12 provide inputs to "word line driver 14 and the NAND gates thereof," which then vary the voltage on word line 58 (which connects to diodes 82, 84). *See* Roberts, column 4, line 38 – column 5, line 6. Thus, Roberts does not and cannot teach or suggest address circuitry comprising a first pattern of rectifiers directly connected between a first set of conductive lines and a first set of address signal lines, as required by amended independent claim 31.

Applicants submit that amended independent claim 31 and claims dependent therefrom are allowable over the cited art for at least these reasons.

CONCLUSION

In light of the foregoing, Applicant respectfully submits that all claims are now in condition for allowance.

A petition for a one-month extension of time is enclosed. The Commissioner is hereby authorized to charge the fee for the extension of time to Deposit Account No. 07-1700. Applicant believes that no additional fees are necessitated by the present Response. However, in the event that any additional fees are due, the Commissioner is hereby authorized to charge any such fees to Deposit Account No. 07-1700.

If the Examiner believes that a telephone conversation with Applicant's agent would expedite allowance of this application, the Examiner is cordially invited to call the undersigned.

Respectfully submitted,

Date: April 24, 2009
Reg. No. 58,533

Electronic Signature: /Matthew T. Currie/
Matthew T. Currie
Agent for the Applicant
Goodwin | Procter LLP
Exchange Place
Boston, Massachusetts 02109

Tel. No.: (617) 570-1198
Fax No.: (617) 523-1231